

SN54AS825A, SN74AS825A 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

- Functionally Equivalent to AMD's AM29825
- Improved I_{OH} Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

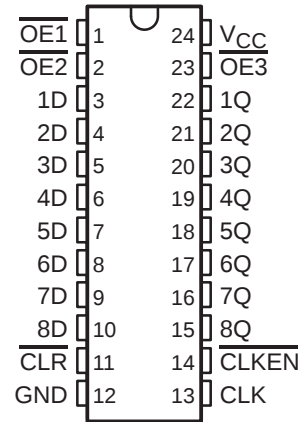
With the clock-enable ($\overline{CLKEN}$) input low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock (CLK) input. Taking $\overline{CLKEN}$ high disables the clock buffer, latching the outputs. These devices have noninverting data (D) inputs. Taking the clear ($\overline{CLR}$) input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-enable ($\overline{OE1}$, $\overline{OE2}$, and $\overline{OE3}$) inputs can be used to place the eight outputs in either a normal logic state (high or low logic level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

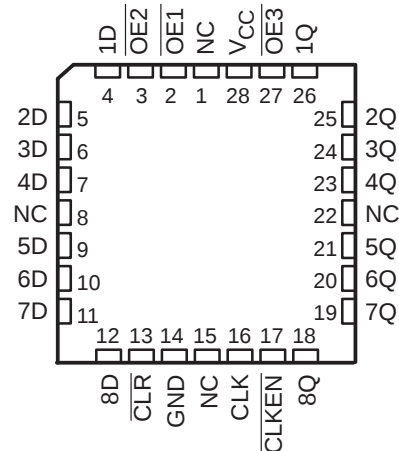
The output enables do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS825A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS825A is characterized for operation from 0°C to 70°C .

SN54AS825A . . . JT PACKAGE
SN74AS825A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS825A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN54AS825A, SN74AS825A

8-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

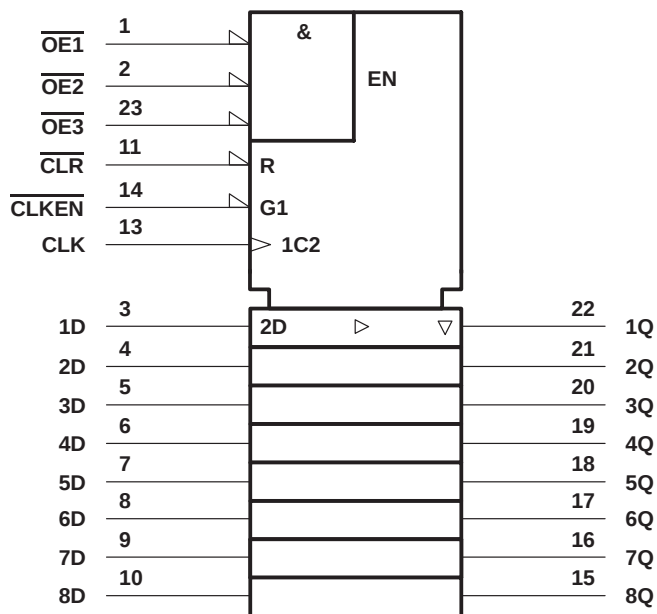
FUNCTION TABLE
(each flip-flop)

INPUTS					OUTPUT Q
$\overline{OE}^\dagger$	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	
L	L	X	X	X	L
L	H	L	$\uparrow$	H	H
L	H	L	$\uparrow$	L	L
L	H	H	X	X	Q ₀
H	X	X	X	X	Z

$^\dagger \overline{OE} = H$ if any of $\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$ are high.

$\overline{OE} = L$ if all of $\overline{OE1}$, $\overline{OE2}$, or $\overline{OE3}$ are low.

logic symbol ‡

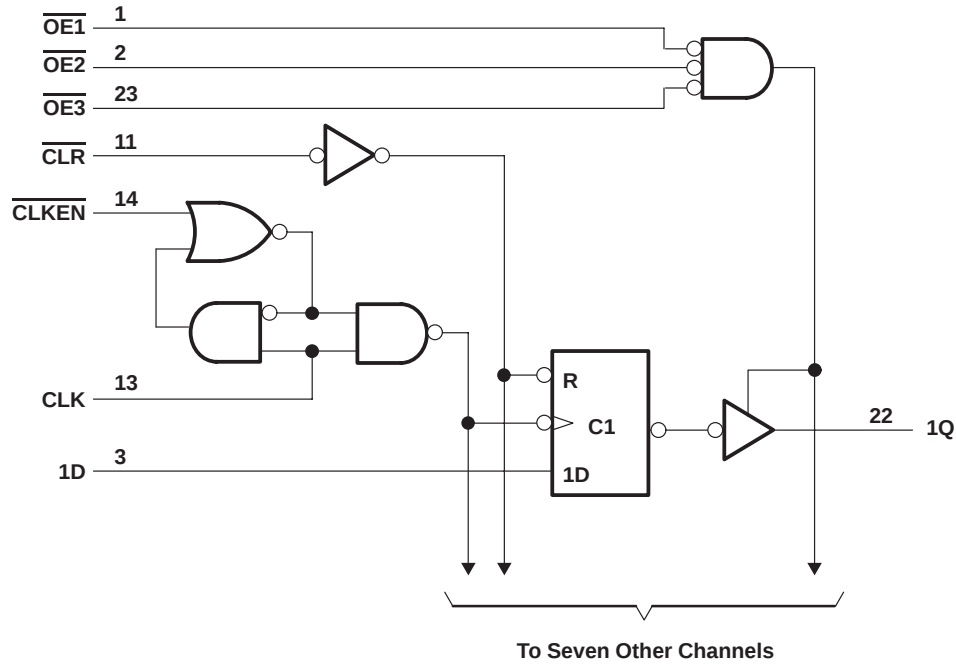


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

SN54AS825A, SN74AS825A 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54AS825A	–55°C to 125°C
SN74AS825A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54AS825A, SN74AS825A

8-BIT BUS-INTERFACE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

recommended operating conditions

			SN54AS825A			SN74AS825A			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage		0.7			0.8			V		
I _{OH}	High-level output current		−24			−24			mA		
I _{OL}	Low-level output current		32			48			mA		
t _w *	Pulse duration	CLR low	7			4			ns		
		CLK high or low	9.5			8					
t _{su} *	Setup time before CLK↑	CLR inactive	8			8			ns		
		Data	7			6					
		CLKEN high or low	10			6					
t _h *	Hold time after CLK↑	CLKEN low or data	0			0			ns		
T _A	Operating free-air temperature		−55			125			0	70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS825A			SN74AS825A			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				–1.2			–1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -2\text{ mA}$		$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -15\text{ mA}$	2.4	3.2		2.4	3.2		
		$I_{OH} = -24\text{ mA}$	2			2			
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 32\text{ mA}$		0.3	0.5				V
		$I_{OL} = 48\text{ mA}$				0.35	0.5		
I_{OZH}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$				50			50	μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$				–50			–50	μA
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$				0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$				20			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$				–0.5			–0.5	mA
$I_O^\ddagger$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$		–30		–112	–30		–112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high		45	73		45	73	mA
		Outputs low		56	90		56	90	
		Outputs disabled		59	95		59	95	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54AS825A, SN74AS825A 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

switching characteristics (see Figure 1)

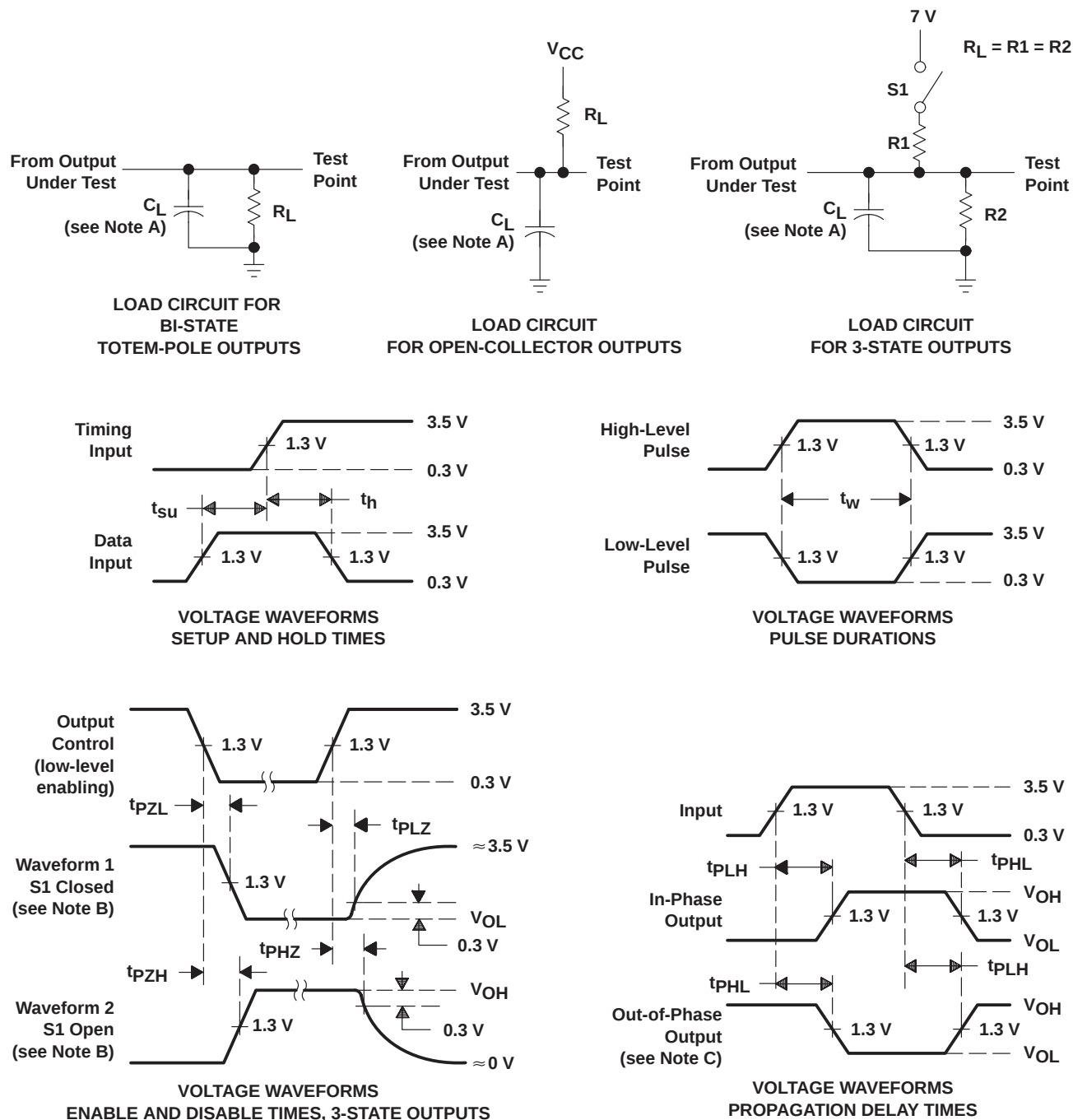
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS825A		SN74AS825A		
			MIN	MAX	MIN	MAX	
t _{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t _{PHL}			3.5	13.5	3.5	13	
t _{PHL}	CLR	Any Q	3.5	16.5	3.5	15.5	ns
t _{PZH}	OE	Any Q	4	12	4	11	ns
t _{PZL}			4	13	4	12	
t _{PHZ}	OE	Any Q	1	10	1.5	8	ns
t _{PLZ}			1	10	1.5	8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54AS825A, SN74AS825A 8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS020B – JUNE 1984 – REVISED AUGUST 1995

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.